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TD-SCDMA BER Performance Designs

The TDSCDMA_BER_wrk workspace demonstrates BER and BLER performance. Three example designs are included in this workspace:

- BER and BLER performance of a 12.2k uplink channel with AWGN: TDSCDMA_12_2_UL_AWGN
- BER and BLER performance of a 12.2k uplink reference fading channel with joint detection receiver: TDSCDMA_12_2_UL_Fading_JD
- BER and BLER performance of a 12.2k downlink fading channel with joint detection receiver: TDSCDMA_12_2_DL_Fading_JD

12.2k Uplink Channel with AWGN

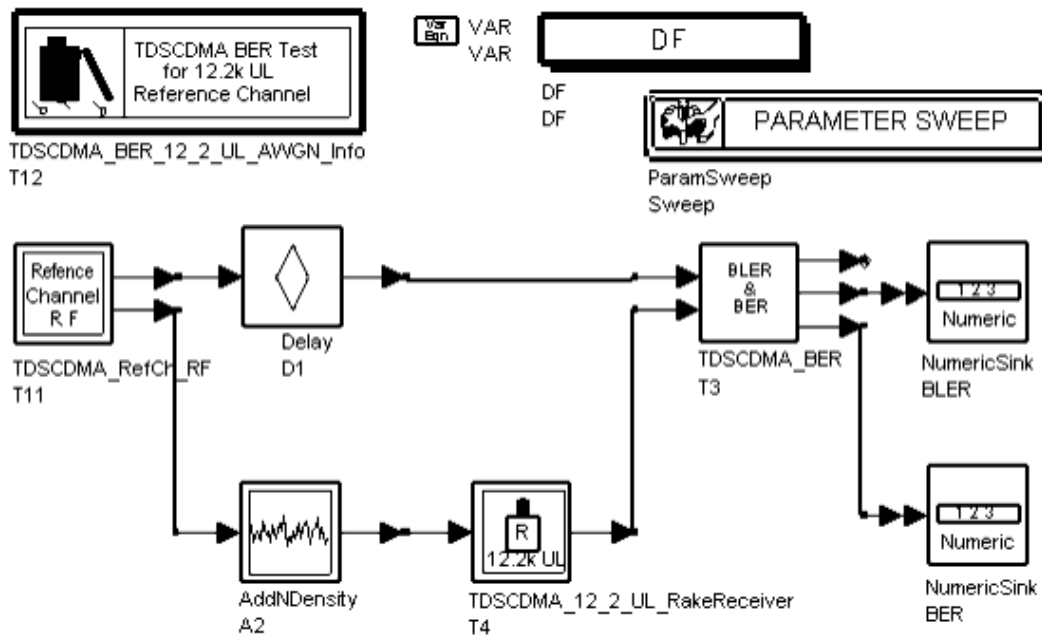
TDSCDMA_12_2_UL_AWGN

Description

BER and BLER performance of a 12.2k uplink channel with AWGN is demonstrated in this design.

The top-level schematic for this design is shown in the following image.

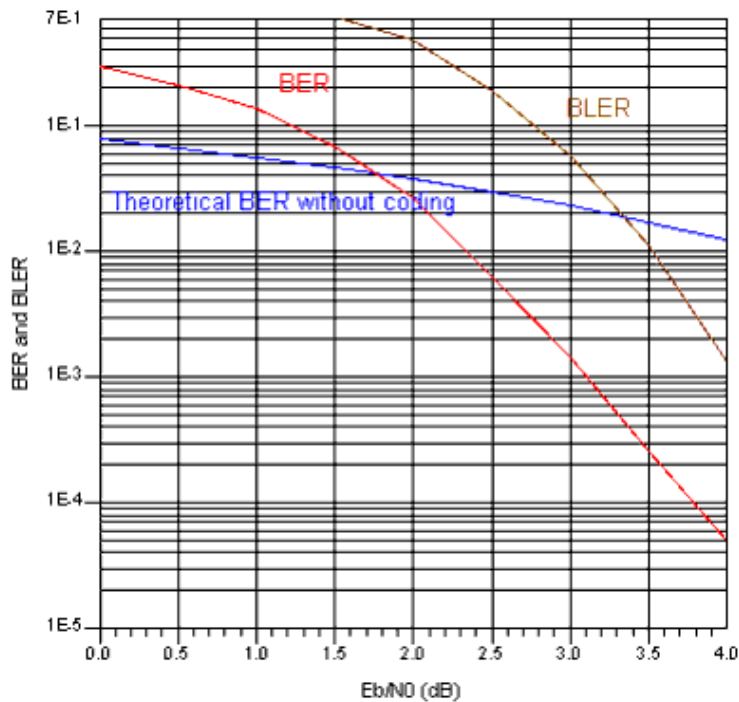
- TDSCDMA_RefCh_RF is used to generate an uplink RF reference measurement channel. One physical channel is used to carry one DCH and one DCCH. The spreading factor is 8.
- A convolution encoder is used. The code rate is 1/3 and the constraint length is 7. A rate match component is placed after the encoder with a 1/3 puncture rate.
- A Rake receiver is applied.



TDSCDMA_12_2_UL_AWGN Schematic

Simulation Results

Simulation results are displayed in the following image.



Simulation Results

Benchmark

- Hardware Platform: Pentium 4 1.8GHz, 512 MB memory
- Software Platform: Windows XP, ADS 2003A
- Simulation Time: 20 hours

References

1. 3GPP Technical Specification TS 25.142 V4.5.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; Base station Conformance (TDD) (Release 4)" June, 2002.

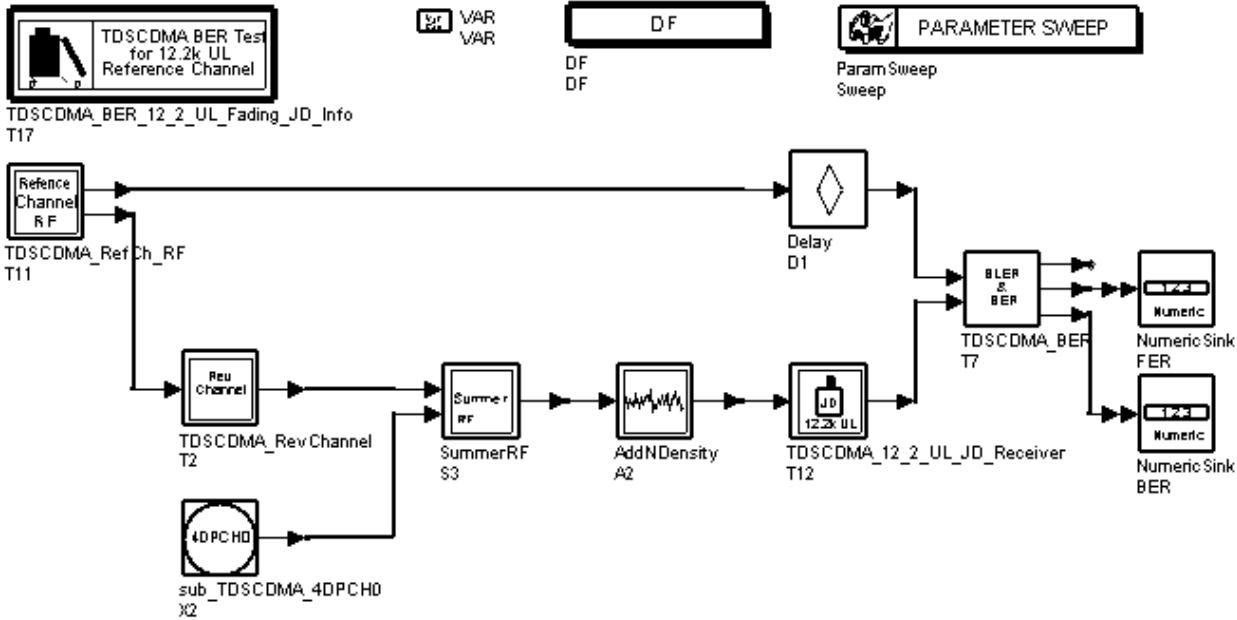
12.2k Uplink Fading Channel with Joint Detection Receiver

TDSCDMA_12_2_UL_Fading_JD

Description

BER and BLER performance of a 12.2k uplink reference fading channel with joint detection receiver is demonstrated in this design.

The top-level schematic for this design is shown in the following image.



TDSCDMA_12_2_UL_Fading_JD Schematic

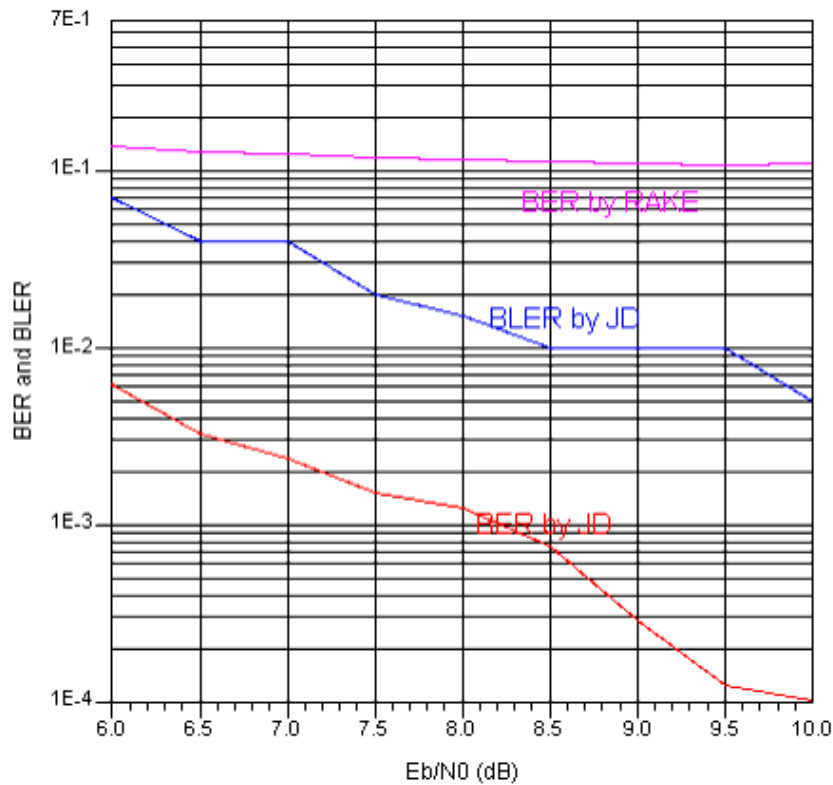
- TDSCDMA_RefCh_RF is used to generate an uplink reference measurement channel. One DPCH is used to carry one DCH and one DCCH. The spreading factor is 8.
- A convolution encoder is used. The code rate is 1/3 and the constraint length is 7. A rate match component is placed after the encoder with a 1/3 puncture rate.
- The following table lists propagation conditions (defined in the reference) for multi-path fading environment performance measurements (Case 3 is applied in this design). All taps have classical Doppler spectrum.

Propagation Conditions for Multi-Path Fading Environments

Case 1, 3 km/hr		Case 2, 3 km/hr		Case 3, 120 km/hr	
Relative Delay (nsec)	Average Power (dB)	Relative Delay (nsec)	Average Power (dB)	Relative Delay (nsec)	Average Power (dB)
0	0	0	0	0	0
2928	-10	2928	0	781	-3
		1200	0	1563	-6
				2344	-9

Simulation Results

Simulation results are displayed in the following image.



Simulation Results

Benchmark

- Hardware Platform: Pentium 4 2.3GHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2003C
- Simulation Time: 60 hours

References

1. 3GPP Technical Specification TS 25.142 V4.5.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; Base station Conformance (TDD) (Release 4)" June, 2002.

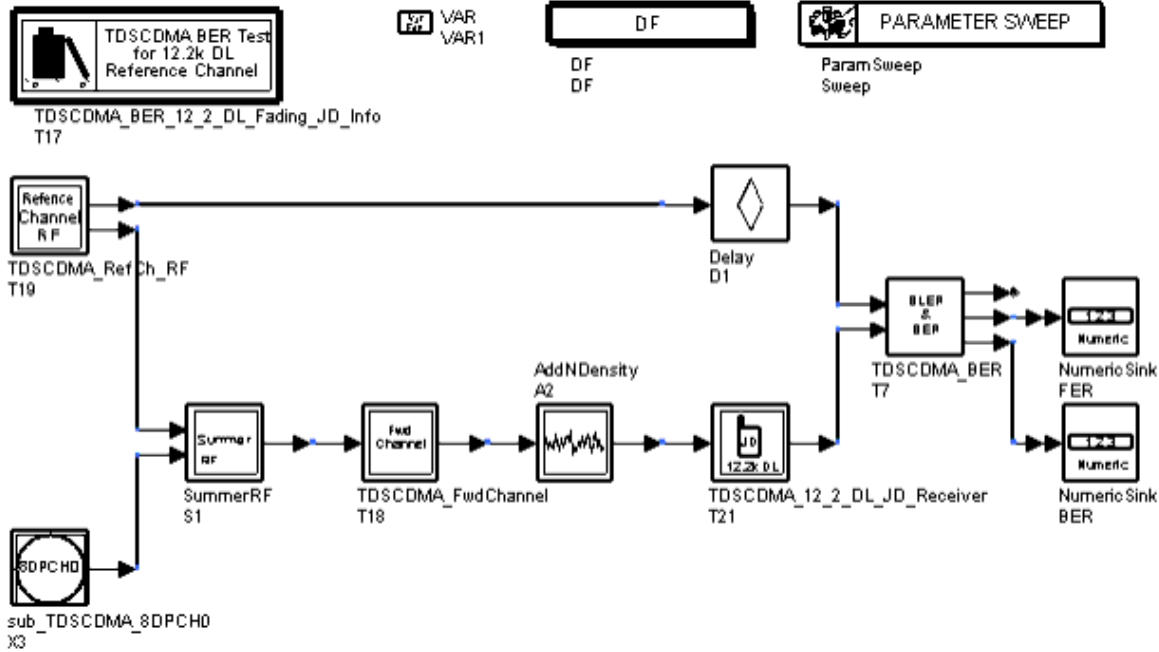
12.2k Downlink Fading Channel

TDSCDMA_12_2_DL_Fading_JD

Description

BER and BLER performance of a 12.2k downlink fading channel with joint detection receiver is demonstrated in this design.

The top-level schematic for this design is shown in the following image.



TDSCDMA_12_2_DL_Fading_JD Schematic

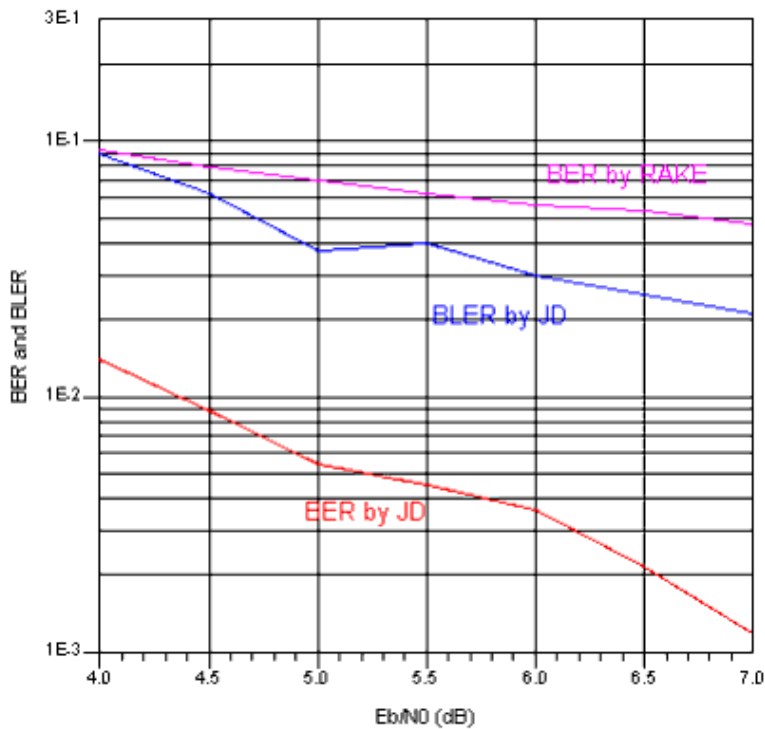
- TDSCDMA_RefCh_RF is used to generate a downlink reference measurement channel. Two DPCHs carry one DCH and one DCCH. The spreading factor is 16.
- A convolution encoder is used. The code rate is 1/3 and the constrain length is 7. A rate matching component is placed after the encoder with a 1/3 puncture rate.
- A joint detection receiver is applied.
- The following table lists propagation conditions (defined in the reference) for multi-path fading environment performance measurements (Case 3 is applied in this design).

Propagation Conditions for Multi-Path Fading Environments

Case 1, 3 km/hr		Case 2, 3 km/hr		Case 3, 120 km/hr	
Relative Delay (nsec)	Average Power (dB)	Relative Delay (nsec)	Average Power (dB)	Relative Delay (nsec)	Average Power (dB)
0	0	0	0	0	0
2928	-10	2928	0	781	-3
		1200	0	1563	-6
				2344	-9

Simulation Results

Simulation results are displayed in the following image.



Simulation Results

Benchmark

- Hardware Platform: Pentium 4 2.3GHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2003C
- Simulation Time: 35 hours

References

1. 3GPP Technical Specification TS 34.122 V4.5.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; Base station Conformance (TDD) (Release 4)" June, 2002.

TD-SCDMA Instrument Link Designs

Introduction

The TD-SCDMA_LinkTest_wrk workspace demonstrates the characteristics of ADS and instrument links. Design examples in this workspace are described in the following sections:

- Base station signal generated using ADS-ESGc link measured by VSA89600: TDSCDMA_DL_Link.
- User equipment signal generated using ADS-ESGc link measured by VSA89600: TDSCDMA_UL_Link.

Base Station

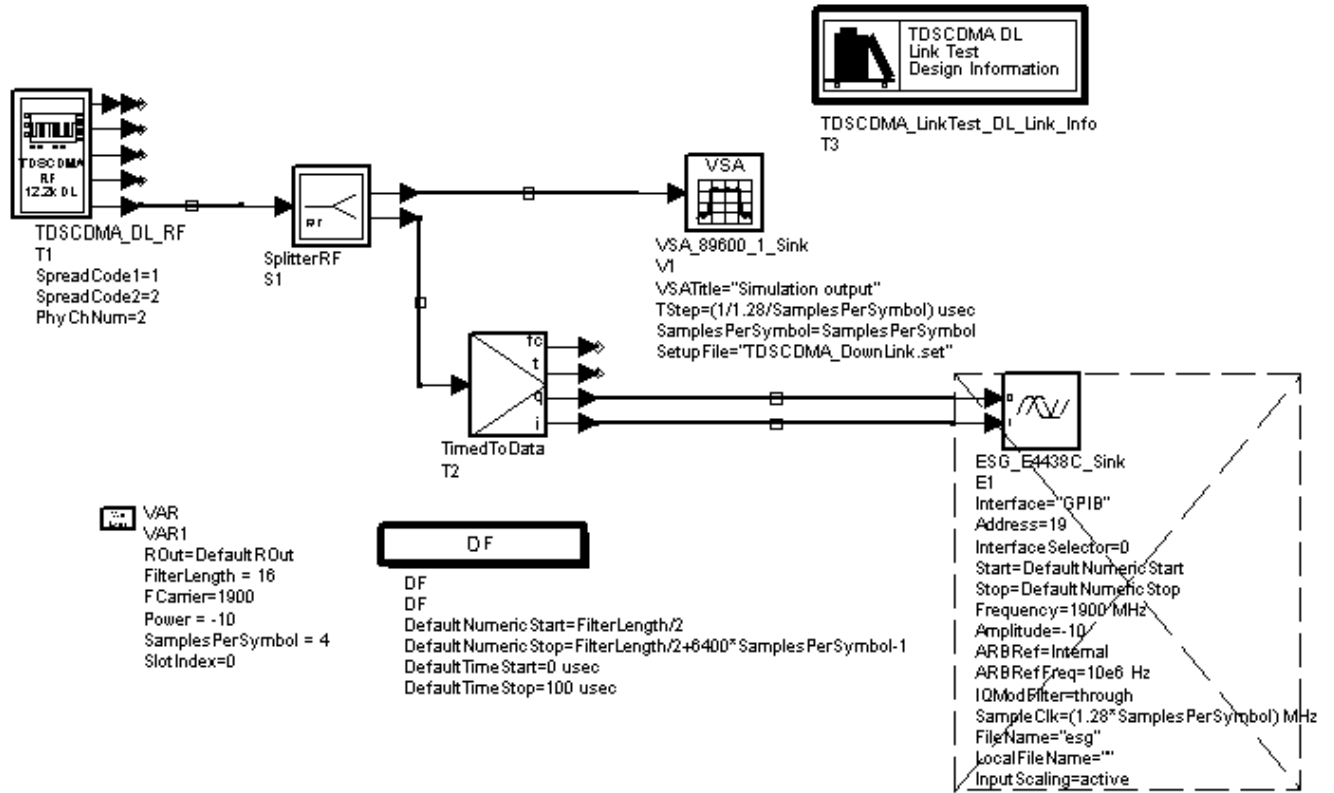
Signal Generated Using ADS-ESGc Link Measured by VSA89600
TDSCDMA_DL_Link

Description

This design demonstrates ADS and instrument links. The BTS signal is generated using ADS-ESGc link, then measured by VSA89600.

The top-level schematic for this design is shown in TDSCDMA_DL_Link Schematic.

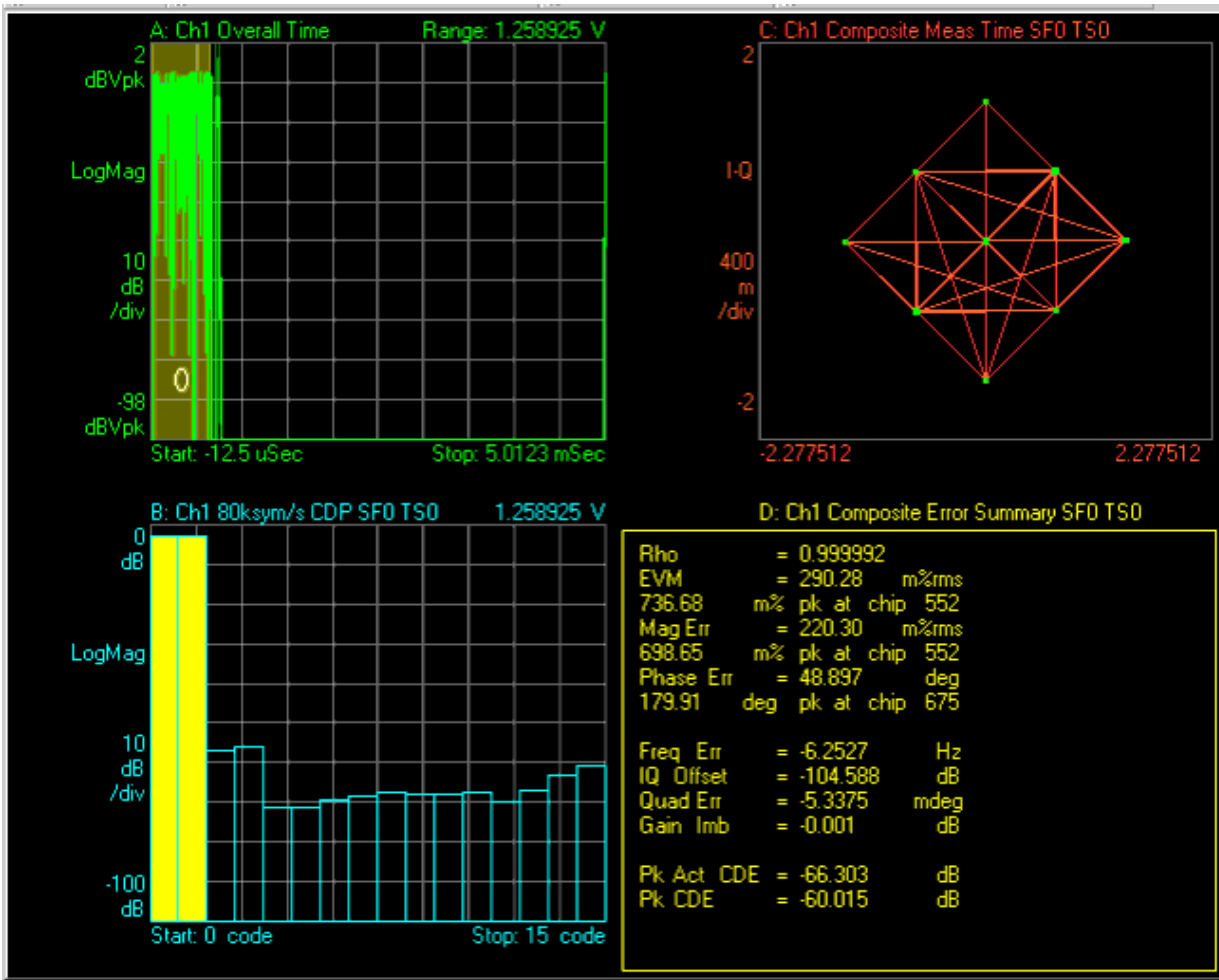
- TDSCDMA_DL_RF is used to generate downlink RF signal.
- VSA_89600_1_Sink is used to start VSA89600 software to measure the RF signal.
- ESG_E4438C_Sink is used to send I, Q data to ESG.



TDSCDMA_DL_Link Schematic

Simulation Results

Simulation results are displayed in VSA89600 window and shown in TDSCDMA_DL_Link Simulation Results.



TDSCDMA_DL_Link Simulation Results

Benchmark

- Hardware Platform: Pentium III 800 MHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2002C, VSA89600 4.00x2_BETA
- Simulation Time: N/A

References

1. 3GPP Technical Specification TS 25.142 V4.5.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; Base station Conformance(TDD) (Release 4)" June, 2002.

User Equipment

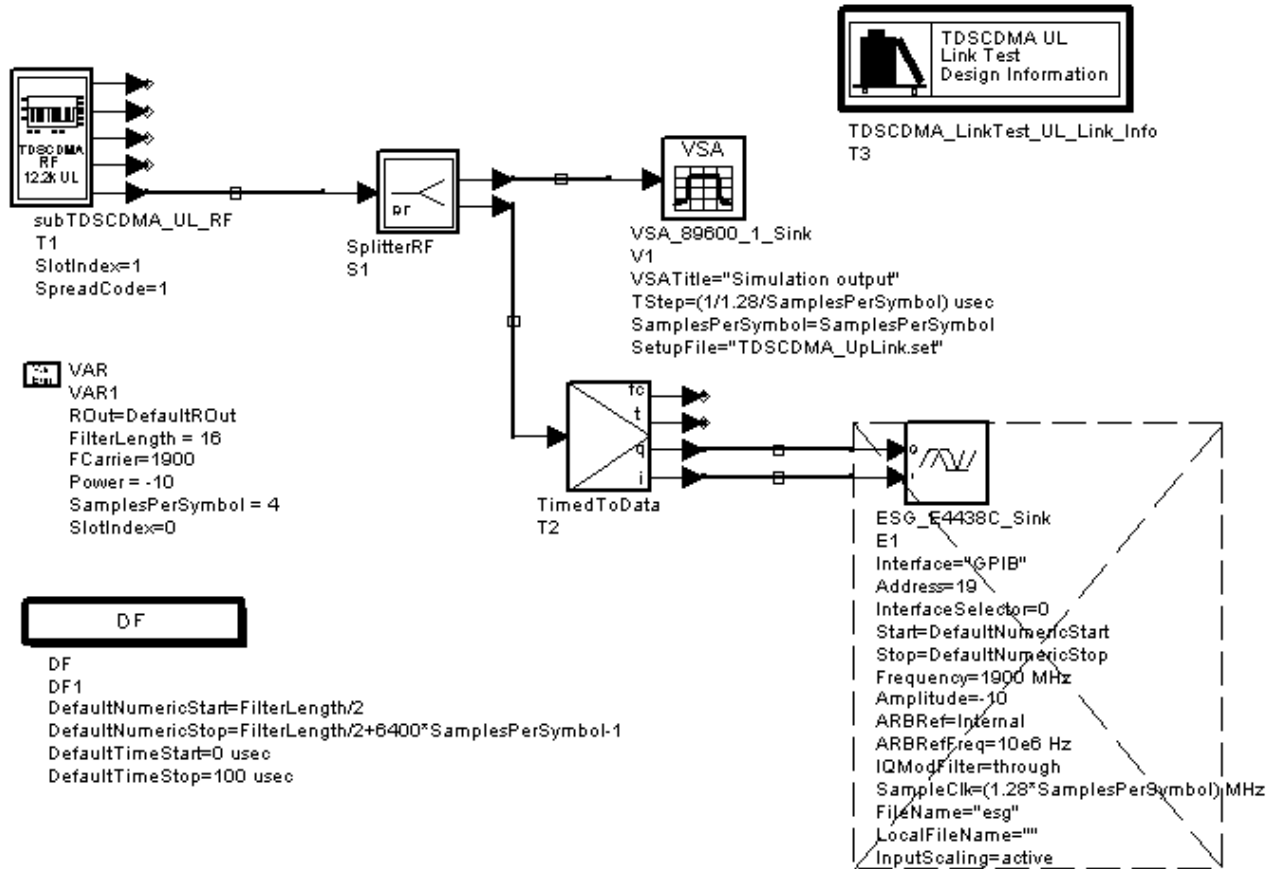
Signal Generated Using ADS-ESGc Link Measured by VSA89600
 TDSCDMA_UL_Link

Description

This design demonstrates ADS and instrument links. The user equipment signal is generated using ADS-ESGc link, then measured by VSA89600.

The top-level schematic for this design is shown in TDSCDMA_UL_Link Schematic.

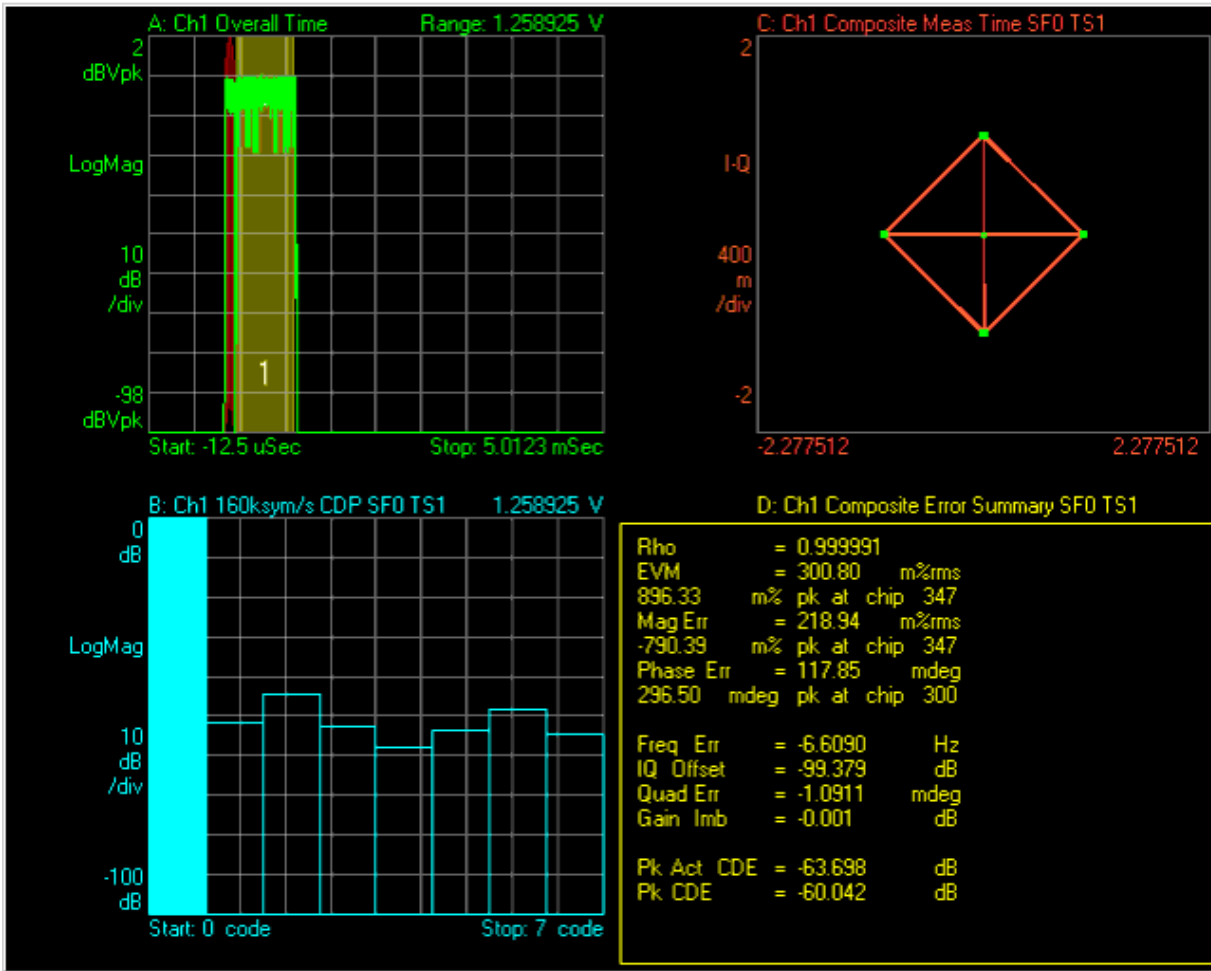
- TDSCDMA_DL_RF is used to generate uplink RF signal.
- VSA_89600_1_Sink is used to start VSA89600 software to measure the RF signal.
- ESG_E4438C_Sink is used to send I, Q data to ESG.



TDSCDMA_UL_Link Schematic

Simulation Results

Simulation results are displayed in VSA89600 window and shown in TDSCDMA_UL_Link Simulation Results.



TDSCDMA_UL_Link Simulation Results

Benchmark

- Hardware Platform: Pentium III 800 MHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2002C, VSA89600 4.00x2_BETA
- Simulation Time: N/A

References

1. 3GPP Technical Specification TS 25.142 V4.5.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; Base station Conformance (TDD) (Release 4)" June, 2002.

TD-SCDMA Power Amplifier Designs

Introduction

The TDSCDMA_PA_Test_wrk workspace includes these design examples.

- Characterization of peak average power ratio versus probability: TDSCDMA_DL_CCDF.
- Instant and average power versus time measurements: TDSCDMA_UL_Power_vs_Time.
- CCDF and spectrum of multi-carrier signal measurements: TDSCDMA_MC_Test.

Complementary

Cumulative Distribution Function Measurements

TDSCDMA_PA_Test_wrk Design Name

- TDSCDMA_DL_CCDF

Features

- Configurable signal source subnetwork model.
- DUT_Gain, FCarrier, Power, SamplesPerSymbol and SlotIndex parameter values can be set by the user.

Description

Complementary cumulative distribution function (CCDF) fully characterizes the power statistics of a signal. It provides peak-average ratio versus probability. The top-level schematic for this design is shown in TDSCDMA_DL_CCDF Schematic.



TDSCDMA_PA_Test_DL_CCDF_Info
Measurement_and_Specification_information



DF
Controller



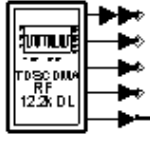
VAR
Signal_Generation_VARS



VAR
RF_Channel_VARS



VAR
Measurement_VARS



TDSCDMA_DL_RF
SignalSource



GainRF
Device_To_Be_Test



TDSCDMA_RF_CCDF
Measurement

TDSCDMA_DL_CCDF Schematic

Simulation Results

Simulation results are displayed in TDSCDMA_DL_CCDF.dds.

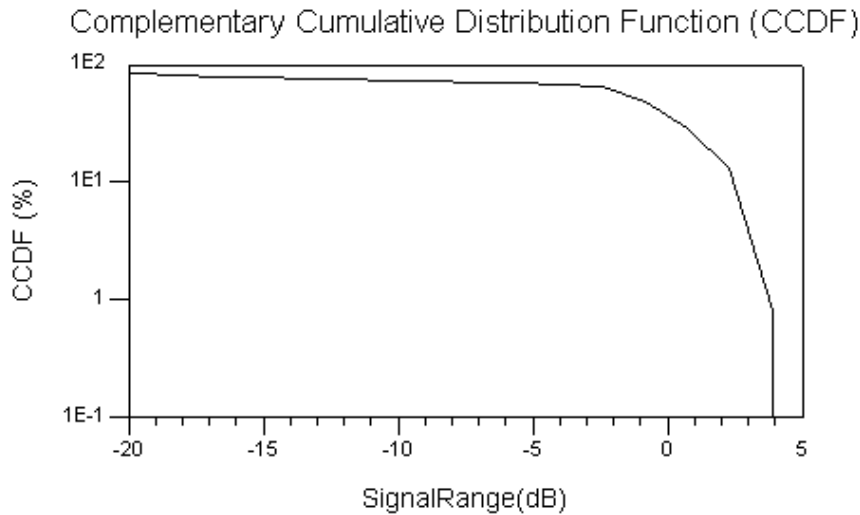
Page main, Page Main of Simulation Results, contains the most important final results and indicates if the measurement results met the requirement of technical specification. In this measurement, the test results would always be passed since there is no requirement of CCDF in TD-SCDMA technical specification.

Page figures, Page Figures of Simulation Results, shows the CCDF curve.

Page equations contains all variable definitions and calculations.

MeanPower(dBm)	PeakPower(dBm)	Peak_to_Mean(dB)
40.115	45.552	5.437

Page Main of Simulation Results



Page Figures of Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 2002
- Simulation Time: approximately 3 minutes

References

1. 3GPP TS 25.221, 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Physical channels and mapping of transport channels onto physical channels onto physical channels (TDD) (Release 4), version 4.3.0, Dec., 2001

Power

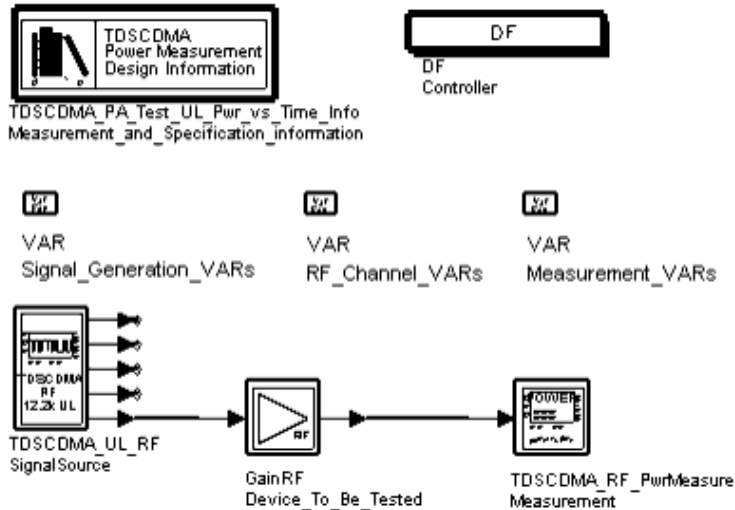
vs. Time Measurement
 TDSCDMA_UL_Power_vs_Time

Features

- Power vs. time measurement
- 12.2kbps uplink reference measurement channel
- Roll-off $\alpha = 0.22$
 root raised-cosine filter

Description

This example measures power vs. time for TD-SCDMA uplink. Power vs. time is calculated by averaging the power of chips at the same position in all measured subframes. The schematic for this design is shown in TDSCDMA_Power_vs_Time Schematic. TDSCDMA_UL_RF generates the 12.2k measurement channel. TDSCDMA_PwrMeasure implements the power measurement.



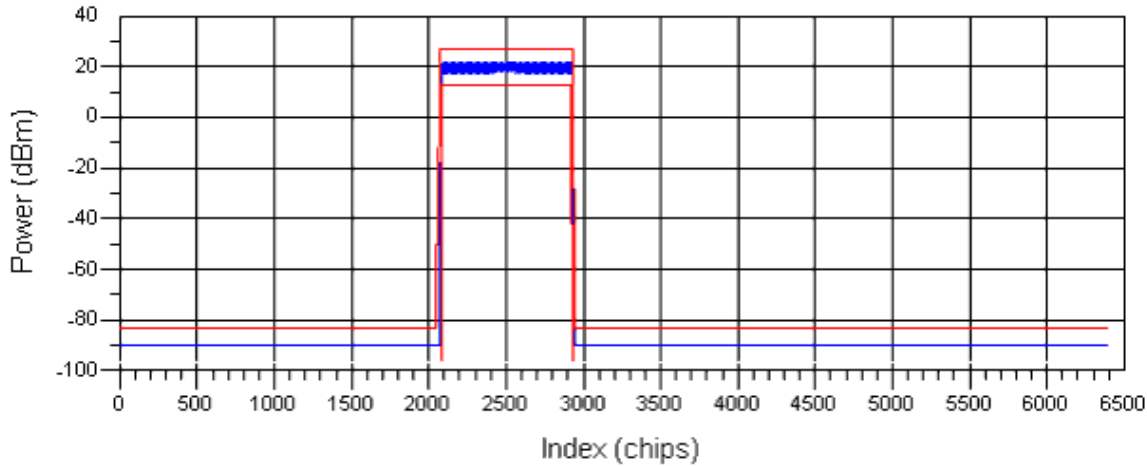
TDSCDMA_Power_vs_Time Schematic

Simulation Results

Simulation results are displayed in Power vs. time for TD-SCDMA Uplink.

The *Equations* page shows the equations that are used for calculating the mask.

TDSCDMA RF Power vs. Time



The test result curves should be within the masks.

Test Results
Passed

Power vs. time for TD-SCDMA Uplink

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2001
- Simulation Time: approximately 2 minutes

References

1. 3GPP TS 25.102, 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; UTRA(UE) TDD; Radio transmission and Reception (Release 4), version 4.3.0, Dec., 2001

CCDF and

Spectrum Measurements of Multi-carrier Signal

TDSCDMA_PA_Test_wrk Design Name

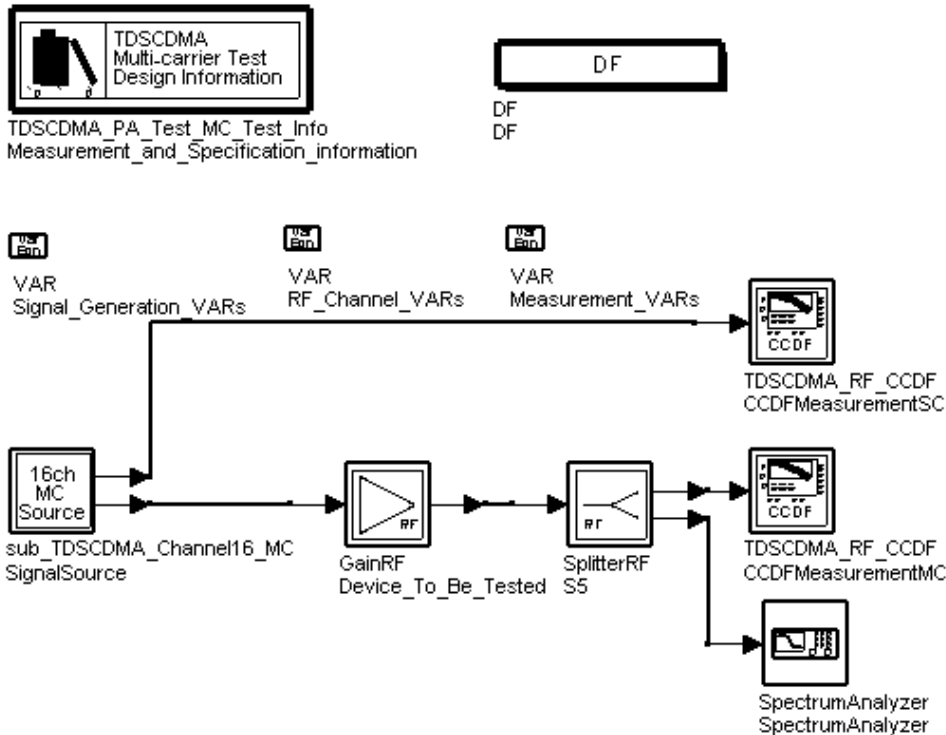
- TDSCDMA_MC_Test

Features

- Multi-carrier signal source with 16 code channels on each carrier.
- FCarrier, FiletrLength, SamplesPerSymbol, DUT_Gain, NumSlotsMeasured and SystemDelay parameter values can be set by the user.

Description

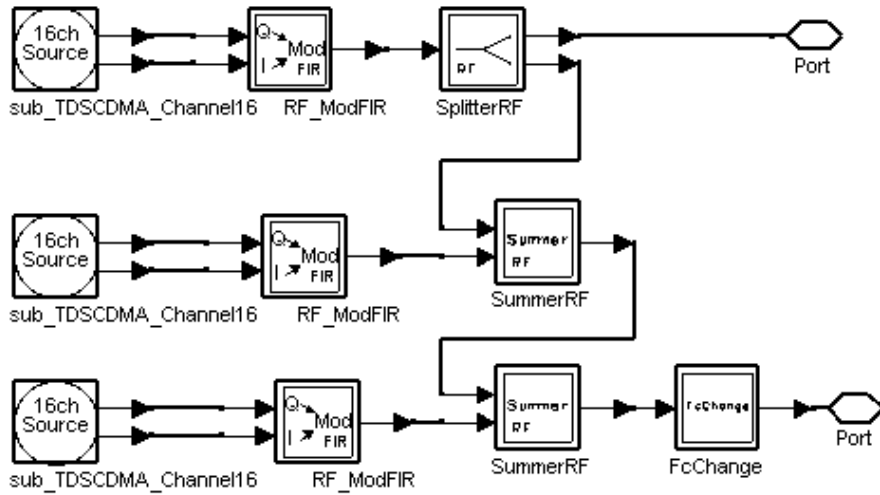
The top-level schematic for this design is shown in TDSCDMA_MC_Test Schematic.



TDSCDMA_MC_Test Schematic

The sub_TDSCDMA_Channel16_MC provides multi-carrier signal on (1900-1.6)MHz, 1900MHz and (1900+1.6)MHz. The CCDFMeasurementMC and SpectrumAnalyzer is used to measure the CCDF and spectrum of the multi-carrier signal and the CCDFMeasurementSC is used to measure the CCDF of the single-carrier signal on 1900MHz.

The sub_TDSCDMA_Channel16_MC schematic is shown in sub_TDSCDMA_Channel16_MC Schematic.

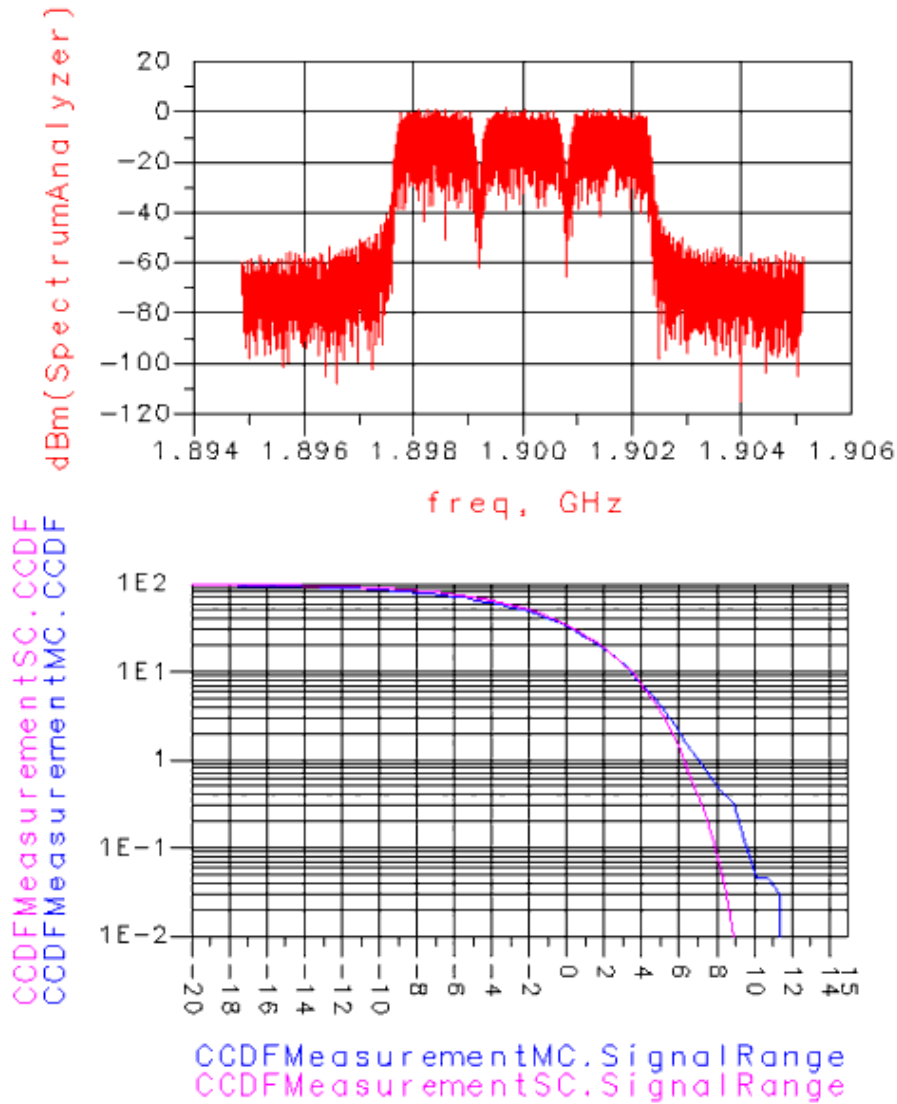


sub_TDSCDMA_Channel16_MC Schematic

X1, X2 and X3 are `sub_TDSCDMA_Channel16` subnetworks which provide baseband signal of a subframe including 16 code channels in time slot 6 and null in other time slots. X1 is modulated to 1900 MHz, X2 to $(1900-1.6)$ MHz and X3 to $(1900+1.6)$ MHz.

Simulation Results

Simulation results displayed in `TDSCDMA_MC_Test.dds` are shown in Simulation Results.



Simulation Results

Benchmark

- Hardware Platform: Pentium III 1 GHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2002
- Simulation Time: approximately 5 minutes

References

1. 3GPP TS 25.221, 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Physical channels and mapping of transport channels onto physical channels onto physical channels (TDD) (Release 4), version 4.3.0, Dec., 2001

TD-SCDMA Receiver Designs

Introduction

The TDSCDMA_Rx_wrk workspace demonstrates user equipment and base station characteristics. Design examples in this workspace are described in the following sections:

- BTS reference sensitivity level: TDSCDMA_UL_Sensitivity.
- UE adjacent channel selectivity: TDSCDMA_DL_AdjacentChannel.

Base Station

Reference Sensitivity Level
TDSCDMA_UL_Sensitivity

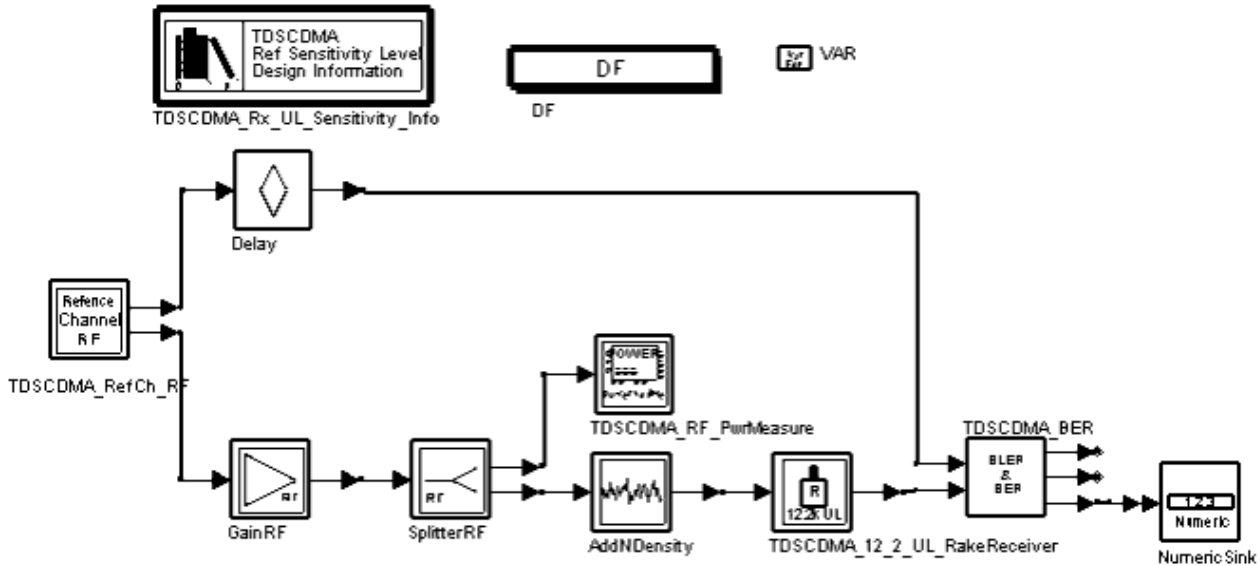
Description

This design measures the base station reference sensitivity level. The reference sensitivity level is the minimum mean power received at the antenna connector at which BER cannot exceed the value given in BS Reference Sensitivity Level.

Reference Measurement Channel Data Rate	BS Reference Sensitivity Level	BER
12.2 kbps	-110 dBm	BER cannot exceed 0.001

The top-level schematic for this design is shown in [TDSCDMA_UL_Sensitivity Schematic](#).

- TDSCDMA_RefCh_RF is used to generate 12.2 kbps uplink RF signal.
- TDSCDMA_12_2_UL_RakeReceiver is used to receive the uplink RF signal with data rate 12.2 kbps.
- TDSCDMA_BER is used to measure the BER
- TDSCDMA_RF_PwrMeasure is used to measure the mean power at the input port of the receiver.



TDSCDMA_UL_Sensitivity Schematic

Simulation Results

Simulation results are displayed in the data display window and shown in TDSCDMA_UL_Sensitivity Simulation Results.

Signal Power :
(dbm)

Index	Average Total Power
1000	-200.000
1001	-200.000
1002	-200.000
1003	-200.000
1004	-200.000
1005	-110.000
1006	-200.000
1007	-200.000
1008	-200.000

Expected: less than 0.1% within 95% confidence

Result:

BER 500	0.000
---------	-------

TDSCDMA_UL_Sensitivity Simulation Results

Benchmark

- Hardware Platform: Pentium III 400 MHz, 512 MB memory
- Software Platform: Windows NT, ADS 2002
- Simulation Time: approximately 6 hours

References

1. 3GPP Technical Specification TS 25.142 V4.5.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; Base station Conformance (TDD) (Release 4)" June, 2002.

User Equipment

Adjacent Channel Selectivity
TDSCDMA_DL_AdjacentChannel

Description

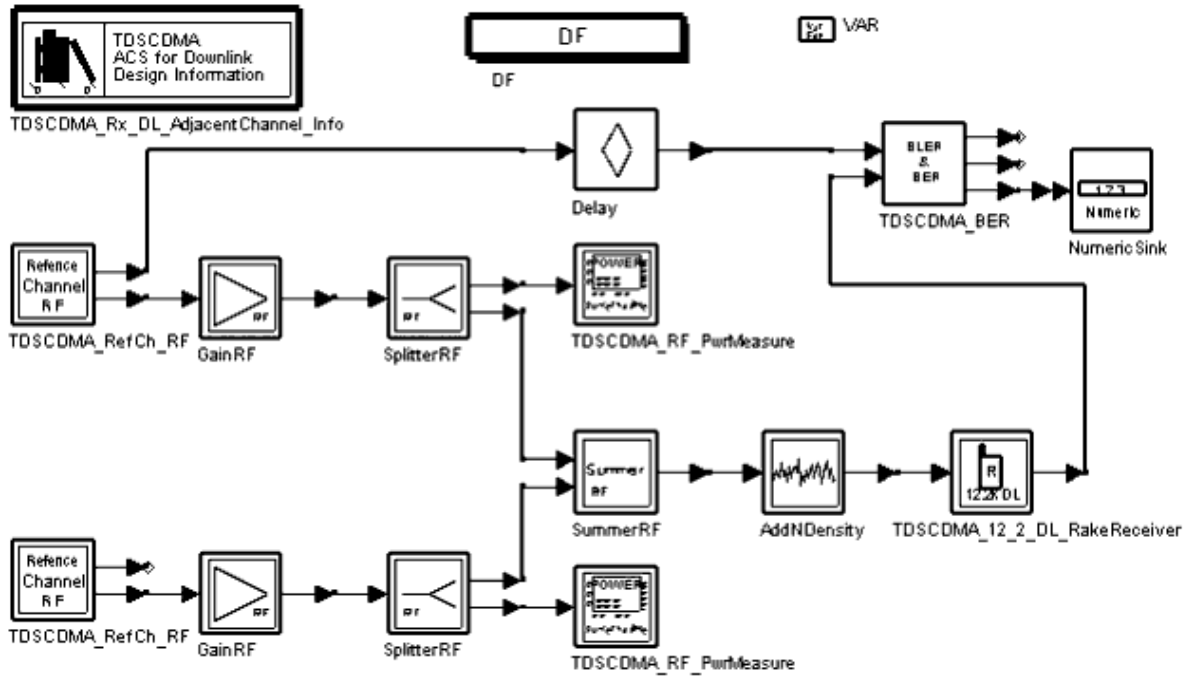
This design measures the adjacent channel selectivity. Adjacent channel selectivity is a measure of the receiver's ability to receive a wanted signal at its assigned channel frequency in the presence of an adjacent channel signal.

For the user equipment power class 2 and 3, the BER cannot exceed 0.001 for parameters specified in Test Parameters for Adjacent Channel Selectivity. This test condition is equivalent to an adjacent channel selectivity value of 33 dB.

Parameter	Unit	Level
$\frac{\Sigma DPCH-E_c}{I_{or}}$	dB	0
I_{or}	dBm/1.28 MHz	-91
I_{osc}	dBm/1.28 MHz	-54
F_{uw} offset	MHz	+1.6 or -1.6

The top-level schematic for this design is shown in TDSCDMA_DL_AdjacentChannel Schematic.

- The upper TDSCDMA_RefCh_RF is used to generate wanted 12.2 kbps downlink RF signal; the lower TDSCDMA_RefCh_RF is the adjacent channel signal.
- TDSCDMA_12_2_DL_RakeReceiver is used to receive the wanted downlink RF signal with a 12.2 kbps data rate in the presence of adjacent channel signal.
- TDSCDMA_BER is used to measure the BER.
- TDSCDMA_RF_PwrMeasure is used to measure the mean power at the input port of the receiver.



TDSCDMA_DL_AdjacentChannel Schematic

Simulation Results

Simulation results are shown in Adjacent Channel Selectivity Measurement Results.

Signal Power :
(dbm)

Index	Signal.AverageTotalPower
1000	-90.998
1001	-200.000
1002	-200.000
1003	-200.000
1004	-200.000
1005	-200.000
1006	-200.000
1007	-200.000
1008	-200.000

Interference Power:
(dbm)

Index	Interference.AverageTotalPower
1000	-53.998
1001	-186.947
1002	-186.941
1003	-186.973
1004	-186.939
1005	-186.943
1006	-186.939
1007	-186.938
1008	-186.948

Expected:

less than 0.1% within 95% confidence

Result:

BER[500]
0.000

Adjacent Channel Selectivity Measurement Results

Benchmark

- Hardware Platform: Pentium III 450MHz, 512MB memory
- Software Platform: Windows 2000, ADS 2002
- Simulation Time: approximately 9 hours

References

1. .3GPP TS 25.122 V4.4.0, "3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Terminal Conformance Specification; Radio transmission and Reception (TDD) (Release 4)", June, 2002

TD-SCDMA Signal Source Designs

Introduction

The TDSCDMA_SignalSource_wrk workspace demonstrates the special transient characteristics of TD-SCDMA signals from time and frequency domains, as well as rate matching calculation. Design examples in this workspace are described in the following sections:

- Uplink signal characteristics: TDSCDMA_UL_Spectrum.
- Downlink signal characteristics: TDSCDMA_DL_ACLR.
- Rate matching calculator demonstration: TDSCDMA_RM_Cal_Demo

Uplink Signal Characteristics

TDSCDMA_UL_Spectrum

Description

This design demonstrates user equipment out-of-band emissions; these are unwanted emissions immediately outside the nominal channel that result from the modulation process and non-linearity in the transmitter but excluding spurious emissions. This out-of-band emission limit is specified in terms of a spectrum emission mask and adjacent channel power.

The spectrum emission mask of the user equipment applies to carrier frequencies that are between 0.8 and 4.0 MHz. The out-of-channel emission is specified relative to the user equipment output power measured in a 1.28 MHz bandwidth. The power of any user equipment emission cannot exceed the levels specified in Spectrum Emission Mask Requirements.

Spectrum Emission Mask Requirements

Δf in MHz†	Minimum Requirements	Measurement Bandwidth
0.8	-35 dBc	30 kHz ††
0.8 - 1.8	$\left\{ -35 - 14 \left(\frac{\Delta f}{\text{MHz}} - 0.8 \right) \right\} \text{dBc}$	30 kHz ††
1.8 - 2.4	$\left\{ -49 - 25 \left(\frac{\Delta f}{\text{MHz}} - 1.8 \right) \right\} \text{dBc}$	30 kHz ††
2.4 - 4.0	-49 dBc	1 MHz †††

† Δf is the separation between the carrier frequency and the center of the measuring filter.

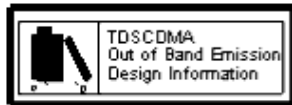
++ The first and last measurement positions with a 30 kHz filter at !dgtdscdma-7-1-05.gif!f equals 0.815 and 2.385 MHz.

+++ The first and last measurement positions with a 1 MHz filter at !dgtdscdma-7-1-06.gif!f equals 2.9 and 3.5 MHz.

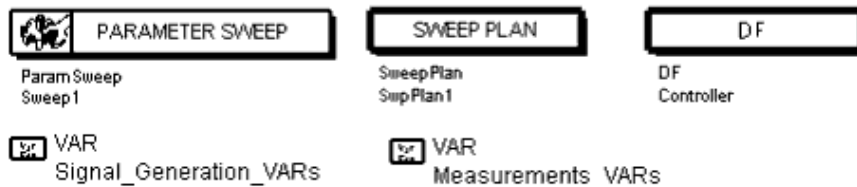
The lower limit must be -55dBm/1.28MHz or the minimum requirement presented in this table, whichever is higher.

The top-level schematic for this design is shown in TDSCDMA_UL_Spectrum Schematic.

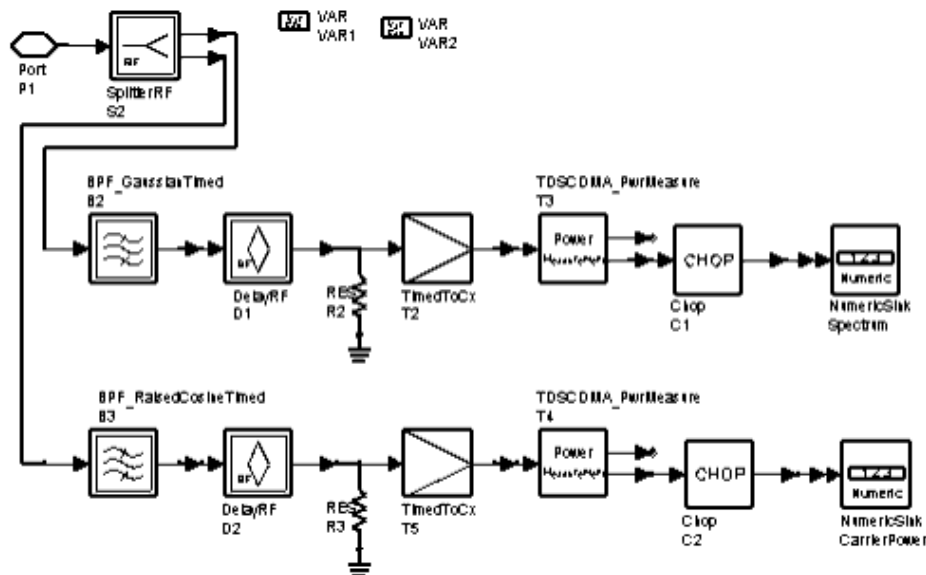
- TDSCDMA_UL_RF generates a 12.2 kbps uplink RF signal source that includes one DPCH.
- The SpectrumMeasure subnetwork, [SpectrumMeasure Subnetwork Schematic](#), measures the out-of-band emission spectrum and the average power measured in a 1.28 MHz bandwidth centered at the carrier frequency.



sub_Spectrum_Info
Measurement_and_Specification_information



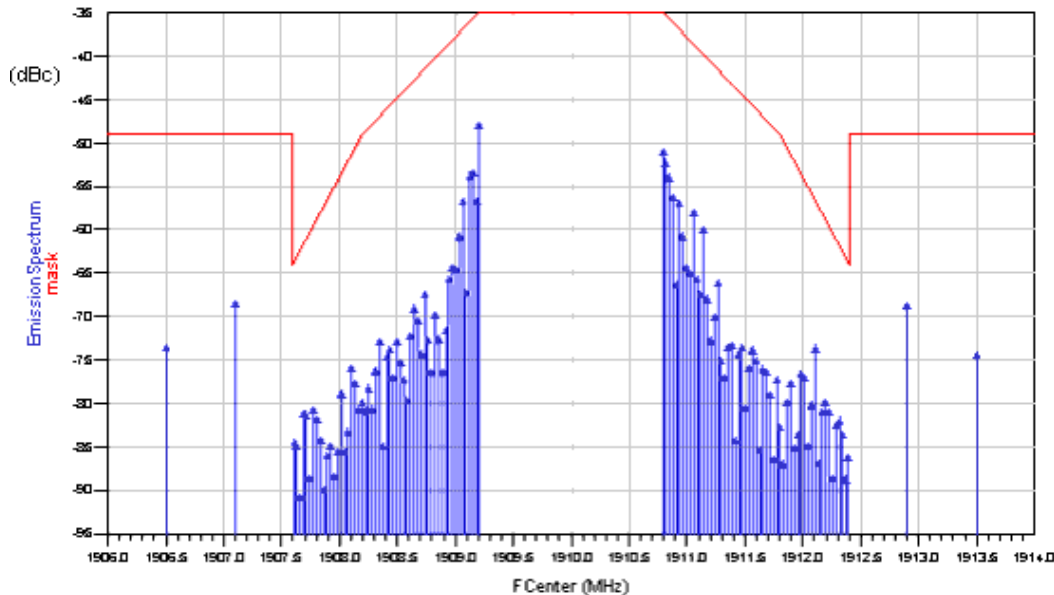
TDSCDMA_UL_Spectrum Schematic



SpectrumMeasure Subnetwork Schematic

Simulation Results

Simulation results displayed in the TDSCDMA_UL_Spectrum.dds data display window are shown in Simulation Results.



Simulation Results

Benchmark

- Hardware Platform: Pentium III 800 MHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2002
- Simulation Time: approximately 1 hour

References

1. 3GPP Technical Specification TS 25.102 V4.2.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; UTRA(UE) TDD; Radio Transmission and Reception (Release 4)" 2000-12.

Adjacent Channel Power Leakage Ratio

TDSCDMA_DL_ACLR

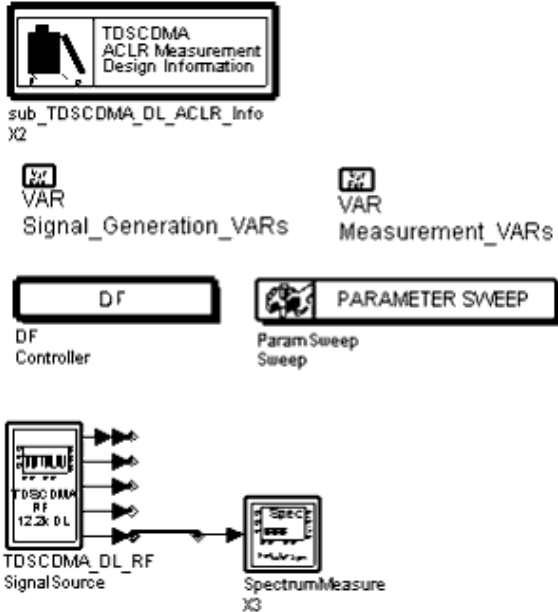
Features

- ACLR measurements for TD-SCDMA downlink
- 12.2 kbps downlink reference measurement channel
- Roll-off $\alpha = 0.22$ root raised-cosine filter

Description

This example measures ACLR for TD-SCDMA downlink.

The schematic for this design is shown in TDSCDMA_DL_ACLR Schematic. TDSCDMA_DL_RF generates the 12.2 kbps downlink reference channel for the measurement. The SpectrumMeasure subnetwork implements average power measurement through a root raised-cosine filter. By offsetting the center frequency of the root raised-cosine filter, power leakage on the adjacent channel is measured.



TDSCDMA_DL_ACLR Schematic

Simulation Results

Simulation results displayed in the TDSCDMA_DL_ACLR.dds data display window are shown in ACLR Measurements for TD-SCDMA Downlink.

FreqOffset	CarrierPower[2,...]-CarrierPower Index=3	
	-3.200	
-1.600		49.925
0.000		0.000
1.600		49.913
3.200		68.300

Notes:
 The ACLR is measured in dB.
 The limits for +/-1.6MHz and +/-3.2MHz offset from the Center Frequency are 40dB and 50dB, respectively, for the minimum requirement.

ACLR Measurements for TD-SCDMA Downlink

Benchmark

- Hardware Platform: Pentium II 400MHz, 523MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002

- Simulation Time: approximately 20 minutes

References

1. 3GPP TS 25.105, 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; UTRA(BS) TDD; Radio transmission and Reception (Release 4), version 4.3.0, Dec., 2001.

Rate Match Calculator

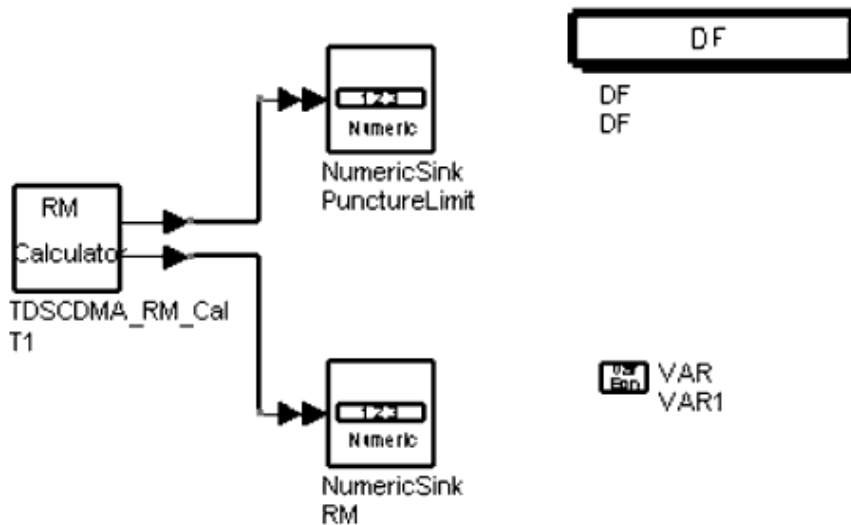
TDSCDMA_RM_Cal_Demo

Description

This design demonstrates the use of TDSCDMA_RM_Cal rate matching calculator model. The puncture limit and rate match attributes are specified by users when they configure TDSCDMA Design Library models related to rate matching.

In TDSCDMA specifications, frame sizes before and after rate matching are supplied for reference measurement channels only. TDSCDMA_RM_Cal calculates the puncture limit and rate match attributes from the given frame sizes.

The schematic for this design is shown in TDSCDMA_RM_Cal_Demo Schematic.



TDSCDMA_RM_Cal_Demo Schematic

Simulation Results

Simulation results displayed in TDSCDMA_RM_Cal_Demo.dds are shown in Puncture Limit and Rate Match for each Transport Channel.

Index	PunctureLimit
0	0.667

Index	RM
0	1.000
1	1.000

Puncture Limit and Rate Match for each Transport Channel

Benchmark

- Hardware Platform: Pentium IV 2.26 GHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2003C
- Simulation Time: 4 seconds

References

1. 3GPP Technical Specification TS 25.222 V4.4.0, Multiplexing and channel coding (TDD) Release 4.

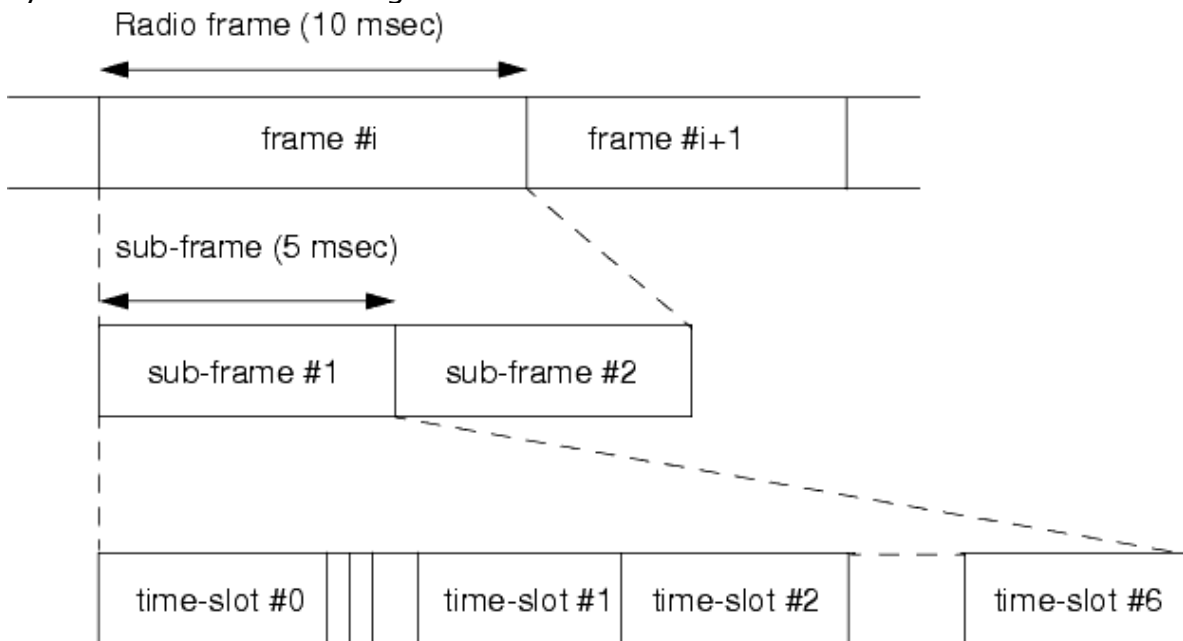
TD-SCDMA Standard

TD-SCDMA is a Chinese contribution to the international family of Mobile Radio Systems for 3G services of UMTS and IMT 2000. It is now one option of UTRA-TDD, called 1.28Mcps TDD or Low Chip Rate (LCR) TDD. It is an advanced CDMA/TDMA/TDD system with an adaptive synchronous operation.

TD-SCDMA system simulation models based on the 3GPP TDD LCR standard demonstrate signal generation capabilities; basic measurements are considered. TD-SCDMA aligns with the same version of the specification used by the Agilent ESG-C, PSA II, and VSA.

Physical Layer

The frame structure in the following illustration recognizes new smart antenna and uplink synchronization technologies.

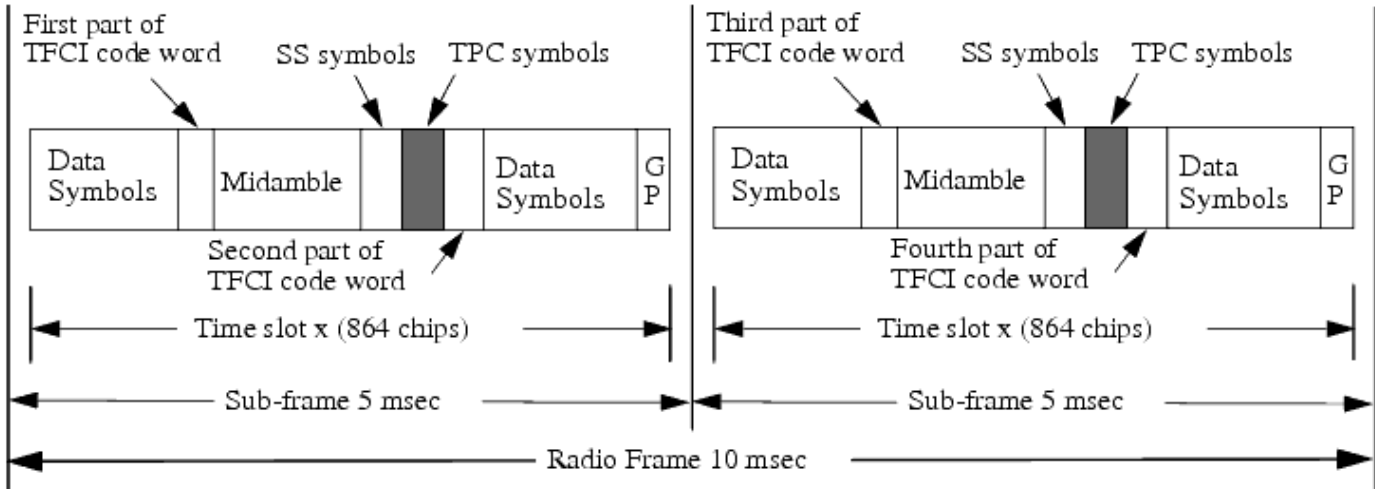


Physical Channel Signal Format

Uplink and downlink time slots in each frame are separated by a switching point. There are two switching points in each sub-frame: TS0 is always allocated as downlink; TS1 is always allocated as uplink. There are three special time slots:

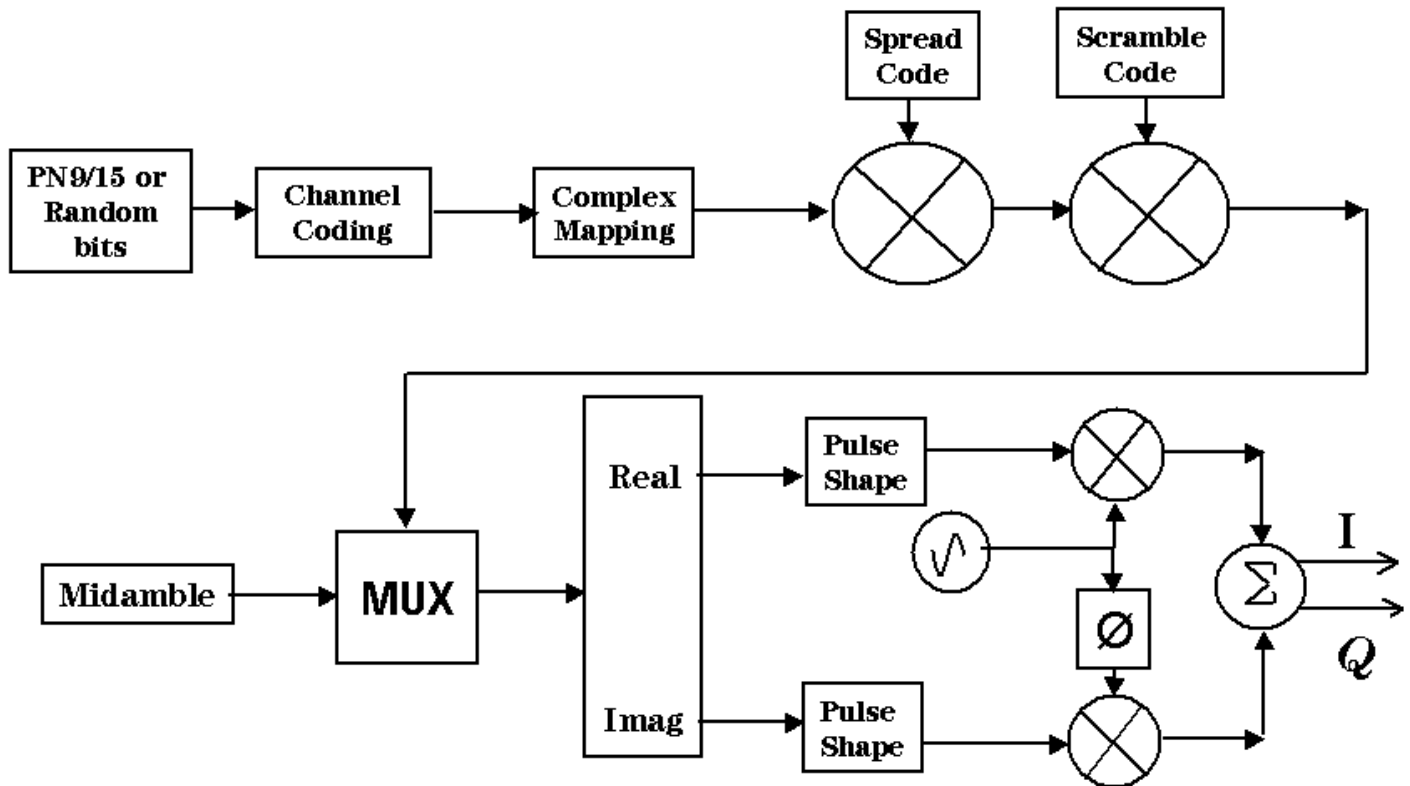
- DwPTS: downlink pilot time slot, 96 chip duration
- UpPTS: uplink pilot time slot, 160 chip duration
- GP: main guard period for TDD operation, 96 chip duration

The system can operate on symmetric and asymmetric modes by properly configuring the number of downlink and uplink time slots. The burst structure is illustrated in the following image.



Burst Structure

The transmitter structure of a physical channel is illustrated in the following image.



Physical Channel Transmitter Structure

There are two kinds of receiver algorithm for TD-SCDMA: Rake and Joint Detection. Physical channels have a 3-layer structure.

- Time slot: 675 usec slot consisting of a number of Symbols. Time slots are used in a TDMA component to separate different user signals in time and code domain.
- Radio frame: 5 msec frame consisting of 7 time slots
- System frame numbering

DesignGuide Examples Overview

Example designs are provided in the **/examples/TDSCDMA** directory. Workspaces and their corresponding design(layout and schematic) examples are:

The TDSCDMA_BER_wrk workspace demonstrates BER and BLER performance.

- BER and BLER performance of a 12.2k uplink channel with AWGN: TDSCDMA_12_2_UL_AWGN
- BER and BLER performance of a 12.2k uplink reference fading channel with joint detection receiver: TDSCDMA_12_2_UL_Fading_JD
- BER and BLER performance of a 12.2k downlink fading channel with joint detection receiver: TDSCDMA_12_2_DL_Fading_JD

The TD-SCDMA_LinkTest_wrk workspace demonstrates the characteristics of ADS and instrument links.

- Base station signal generated using ADS-ESGc link measured by VSA89600: TDSCDMA_DL_Link.
- User equipment signal generated using ADS-ESGc link measured by VSA89600: TDSCDMA_UL_Link.

The TDSCDMA_PA_Test_wrk workspace includes these design examples.

- Characterization of peak average power ratio versus probability: TDSCDMA_DL_CCDF.
- Instant and average power versus time measurements: TDSCDMA_UL_Power_vs_Time.
- CCDF and spectrum of multi-carrier signal measurements: TDSCDMA_MC_Test.

The TDSCDMA_Rx_wrk workspace demonstrates user equipment and base station characteristics.

- BTS reference sensitivity level: TDSCDMA_UL_Sensitivity.
- UE adjacent channel selectivity: TDSCDMA_DL_AdjacentChannel.

The TDSCDMA_SignalSource_wrk workspace demonstrates the special transient characteristics of TD-SCDMA signals from time and frequency domains.

- Uplink signal characteristics: TDSCDMA_UL_Spectrum.
- Downlink signal characteristics: TDSCDMA_DL_ACLR.

The TDSCDMA_Tx_wrk workspace demonstrates user equipment and base station characteristics.

- Base station error vector magnitude: TDSCDMA_DL_EVM.
- User equipment code domain power: TDSCDMA_UL_CDP.

TD-SCDMA Transmitter Designs

Introduction

The TDSCDMA_Tx_wrk workspace demonstrates user equipment and base station characteristics. Design examples in this workspace are described in the following sections:

- Base station error vector magnitude: TDSCDMA_DL_EVM.
- User equipment code domain power: TDSCDMA_UL_CDP.

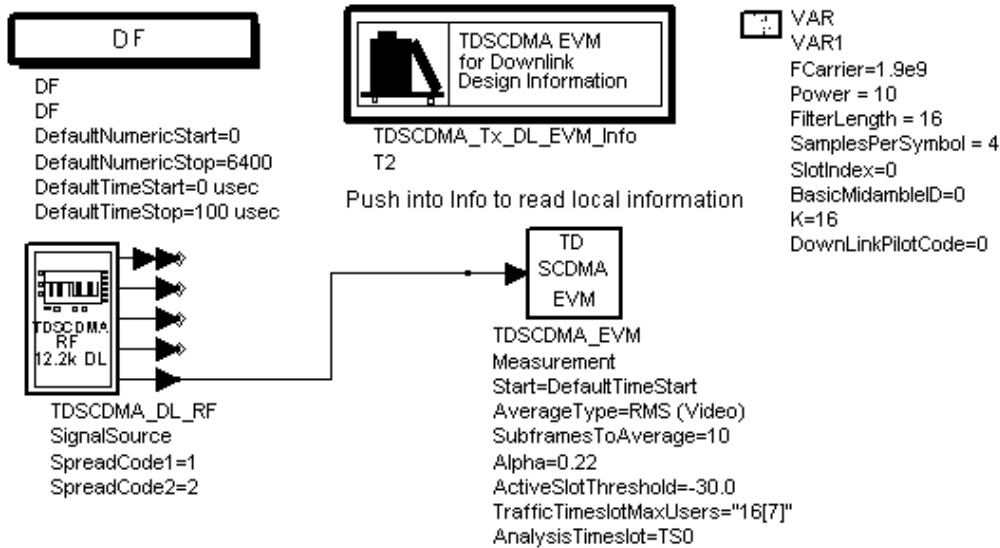
Base Station Error Vector Magnitude

TDSCDMA_DL_EVM

Description

This design demonstrates the base station error vector magnitude measurement to determine the difference between the reference waveform and the measured waveform. This difference is called the error vector. Both waveforms pass through a matched root raised-cosine filter with a bandwidth corresponding to the considered chip rate and roll-off $\alpha = 0.22$. Both waveforms are then further modified by selecting the frequency, absolute phase, absolute amplitude and chip clock timing so as to minimize the error vector. The EVM result is defined as the square root of the ratio of the mean error vector power to the mean reference power expressed as a percentage. The measurement interval is one time slot. The error vector magnitude (EVM) cannot exceed 12.5%. The requirement is valid over the total power dynamic range as specified in subclause 6.4.3 of TS 25.105. The top-level schematic for this design is shown in TDSCDMA_DL_EVM schematic.

- TDSCDMA_DL_RF is used to generate a 12.2 kbps uplink RF signal.
- TDSCDMA_EVM is used to measure the EVM value of the RF signal. The algorithm is the same as that of VSA89600.



TDSCDMA_DL_EVM schematic

Simulation Results

Simulation results are shown in TDSCDMA_DL_EVM Simulation Results.

Average Channel Results

Avg_ChEVMrms_pct	...	Avg_ChMagErr_rms_pct	...	Avg_ChPhaseErr_deg
0.358		0.221		0.157

Channel Results vs Subframe

Subframe	ChEVMrms_pct	ChEVM_Pk_pct	ChEVM_Pk_symbol_idx
1	1.178	2.024	29.000
2	0.234	0.486	21.000
3	0.360	0.632	8.000
4	0.150	0.306	24.000
5	0.427	0.680	21.000
6	0.079	0.178	22.000

Subframe	ChMagErr_rms_pct	ChMagErr_Pk_pct	ChMagErr_Pk_symbol_idx
1	0.828	1.718	43.000
2	0.061	-0.144	40.000
3	0.262	0.518	1.000
4	0.064	0.128	16.000
5	0.284	0.669	8.000
6	0.035	0.085	26.000

Subframe	ChPhaseErr_deg	ChPhaseErr_Pk_deg	..PhaseErr_Pk_symbol_idx	ChCodePhase_deg
1	0.480	-1.135	29.000	0.053
2	0.129	0.276	21.000	0.024
3	0.142	-0.344	38.000	-1.665E-4
4	0.080	0.175	24.000	-0.018
5	0.163	-0.363	21.000	-0.025
6	0.041	0.101	22.000	-0.001

Average Composite Results

Avg_CompEVMrms_pct	...	Avg_CompMagErr_rms_pct	...	Avg_CompPhaseErr_deg
0.371		0.237		35.363

Avg_Rho	Avg_FreqError_Hz
1.000	-0.112

Avg_IQ_Offset_dB	Avg_GuardErr_deg	Avg_GainIrb_dB
-80.791	-0.024	0.001

Composite Results vs Subframe

Subframe	CompEVMrms_pct	CompEVM_Pk_pct	CompEVM_Pk_chip_idx
1	0.749	1.384	40.000
2	0.293	0.636	312.000
3	0.371	0.683	136.000
4	0.265	0.636	195.000
5	0.363	0.650	561.000
6	0.298	0.660	306.000

Subframe	CompMagErr_rms_pct	CompMagErr_Pk_pct	CompMagErr_Pk_chip_idx
1	0.402	1.165	772.000
2	0.218	0.588	312.000
3	0.226	0.610	820.000
4	0.205	0.559	710.000
5	0.236	0.753	244.000
6	0.226	0.608	306.000

Subframe	CompPhaseErr_deg	CompPhaseErr_Pk_deg	..mpPhaseErr_Pk_chip_idx
1	14.326	-1.48332	795.000
2	52.666	-1.78697	51.000
3	26.165	1.78193	320.000
4	34.773	-1.63831	273.000
5	26.876	1.78003	333.000
6	36.336	-1.79362	646.000

Subframe	Rho	FreqError_Hz	IQ_Offset_dB	GuardErr_deg	GainIrb_dB
1	1.000	15.509	-79.688	-0.164	0.004
2	1.000	13.177	-98.513	-0.017	0.002
3	1.000	-0.962	-96.936	0.008	-4.956E-4
4	1.000	-6.523	-93.747	0.002	0.001
5	1.000	-6.021	-99.119	-0.011	3.217E-4
6	1.000	-3.629	-104.650	-0.001	0.001

TDSCDMA_DL_EVM Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0, ADS 2003A
- Simulation Time: 1 minute

References

1. 3GPP Technical Specification TS 25.142 V4.5.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; Base station Conformance (TDD) (Release 4)" June, 2002.

User Equipment Code Domain Power

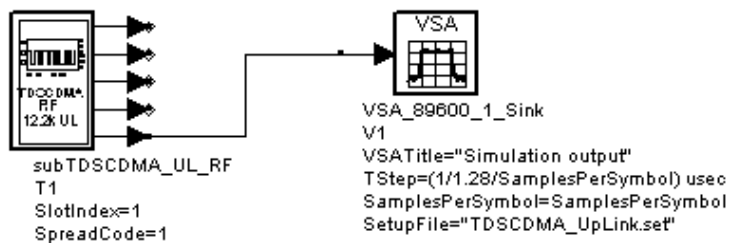
TDSCDMA_UL_CDP

Description

This design demonstrates the code domain power measurement of user equipment. Code domain power is the part of the mean power which correlates with a particular (OVSF) code channel. The sum of all powers in the code domain equals the mean power in a bandwidth of $(1 + \alpha)$ times the chip rate of the radio access mode.

The top-level schematic for this design is shown in TDSCDMA_UL_Link Schematic.

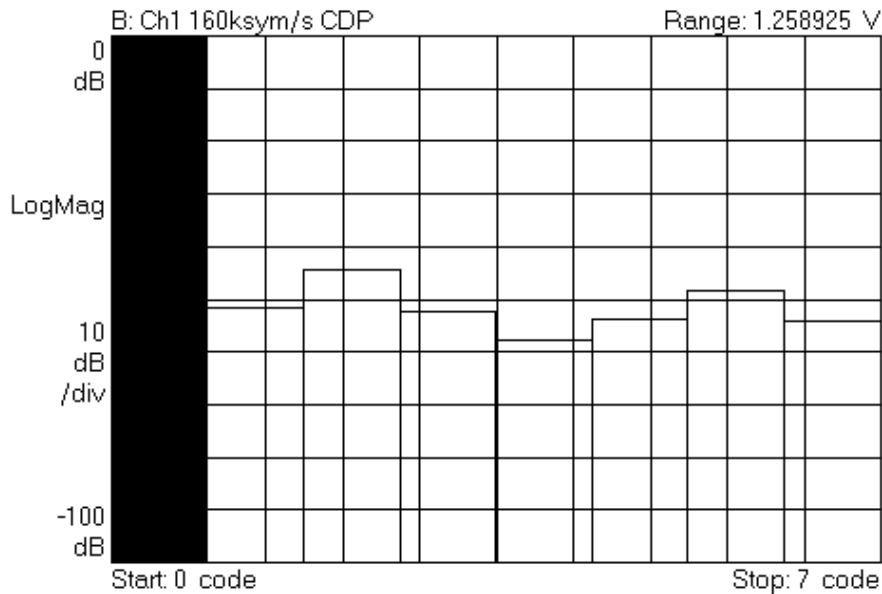
- TDSCDMA_DL_RF is used to generate an uplink RF signal.
- VSA_89600_1_Sink is used to start the VSA89600 software to measure the RF signal.
- ESG_E4438C_Sink is used to send I, Q data to ESG.



TDSCDMA_UL_Link Schematic

Simulation Results

Simulation results are displayed in a VSA89600 window are shown in TDSCDMA_UL_Link Simulation Results.



TDSCDMA_UL_Link Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT4.0, ADS 2002C, VSA89600 4.00x2_BETA
- Simulation Time: 1 minute

References

1. 3GPP Technical Specification TS 25.142 V4.5.0 "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; Base station Conformance (TDD) (Release 4)" June, 2002.